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EXAMINER	
TORRES, JUAN A	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/997,655	KWASAKI ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14 and 15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/15/2007 has been entered.

Response to Arguments

Regarding claims 1, 14 and 15:

Applicant's arguments filed on 03/15/2007 have been fully considered but they are not persuasive.

The Applicant contends, "In other words, a combination of Solheim et al., Wada and Turney, even if obvious to one skilled in file art at the time the claimed invention was made, would still have failed to disclose or suggest, "[a] transmission device performing a signal regeneration control, comprising: a clock timing extraction circuit dynamically setting a frequency-dividing ratio based on a transmission rate of an input signal to perform a phase synchronization control so that the input signal and an oscillation output have a constant phase difference and extracting a clock timing based on the transmission rate; and a regeneration control circuit sequentially sweeping a voltage threshold level and a phase of an extracted clock with respect to the input signal to determine whether signal logic levels measured at adjacent monitor points match with

each other and to automatically measure a decision point within a valid zone of an eye pattern at which there is the least possibility that error occurs and performing the regeneration control by using the decision point as an optimal point, wherein the regeneration control circuit performs said sweeping of the voltage threshold level and the phase or the extracted clock at intervals derived from a target error rate of the input signal," as recited in claim 1 (emphasis in original).

The Examiner disagrees and asserts, that, Solheim discloses that the regeneration control circuit performs the sweeping of the voltage threshold level and the phase of the extracted clock at intervals derived from a target error, rate of the input signal (column 6 lines 40-46). Specifically Solheim discloses "FIG. 4A is a flow chart of the operation of the control circuit in the error mapping mode. After control circuit 16 assumes the error mapping mode of operation, as shown in step 100, the threshold V_{th} and the phase Φ are initialized for BER contour mapping in step 101. T_{prov} defines the sampling time for measuring the current raw BER. Alternatively, rather than measuring the true current BER_{raw}, a shorter time interval T_{prov} may be set for limiting the collection time for each pair (V_i,. Φ_j). T_{prov} should be selected long enough to obtain a raw BER which is below the maximum admissible error rate BER_{prov}. Steps 102 to 108 illustrate the mapping process, wherein the slicing level V_i takes (I) successive values, and the phase Φ_j takes (J) successive values. In the example shown in FIG. 2, I=10 and J=16. All pairs (V_i,. Φ_j) are applied to the comparator 10 and flip-flop 12, respectively, in step 102, and the current raw BER is measured in step 103 for the time interval T_{prov}, as illustrated in step 104" (emphasis added).

For these reasons and the reason stated en the previous Office action, the rejection of claims 1, 14 and 15 are maintained.

Regarding claims 2-12:

Applicant's arguments filed on 03/15/2007 have been fully considered but they are not persuasive.

The Applicant contends, "

Accordingly, Applicants respectfully submit that claim 1, together with claims 2, 5-12, and 16 dependent therefrom, is patentable over Solheim et al., Wada, and Turney, separately and in combination, for at least the foregoing reasons".

The Examiner disagrees and asserts, that, because the rejection of claim 1 is maintained, the rejections of claims 2-12 are also maintained.

For these reasons and the reason stated en the previous Office action, the rejection of claims 2-12 are maintained.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 5-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Solheim (US 5896391) in view of Turney (US 4516083 A), and further in view of Wada (US 5602879 A).

As per claim 1, Solheim discloses a regeneration control circuit sequentially sweeping a voltage threshold level and a phase of an extracted clock with respect to the input signal (figure 3 column 5 line 25 to column 6 line 35); and that the regeneration control circuit performs the sweeping of the voltage threshold level and the phase of the extracted clock at intervals derived from a target error, rate of the input signal (column 6 lines 40-46. Specifically Solheim discloses "FIG. 4A is a flow chart of the operation of the control circuit in the error mapping mode. After control circuit 16 assumes the error mapping mode of operation, as shown in step 100, the threshold V_{th} and the phase Φ are initialized for BER contour mapping in step 101. T_{prov} defines the sampling time for measuring the current raw BER. Alternatively, rather than measuring the true current BER_{raw}, a shorter time interval T_{prov} may be set for limiting the collection time for each pair (V_i,. Φ_j). T_{prov} should be selected long enough to obtain a raw BER which is below the maximum admissible error rate BER_{prov}. Steps 102 to 108 illustrate the mapping process, wherein the slicing level V_i takes (I) successive values, and the phase Φ_j takes (J) successive values. In the example shown in FIG. 2, I=10 and J=16. All pairs (V_i,. Φ_j) are applied to the comparator 10 and flip-flop 12, respectively, in step 102, and the current raw BER is measured in step 103 for the time interval T_{prov}, as illustrated in step 104"). Solheim doesn't disclose a clock timing extraction circuit dynamically setting a frequency-dividing ratio based on a transmission rate of an input signal to perform a phase synchronization control so that the input signal and an oscillation output have a constant phase difference and extracting a clock timing based on the transmission rate; and determine whether signal logic levels measured at adjacent monitor points match

with each other and to automatically measure a decision point within a valid zone of an eye pattern at which there is the least possibility that error occurs and performing the regeneration control by using the decision point as an optimal point. Turney discloses a clock timing extraction circuit dynamically setting a frequency-dividing ratio based on a transmission rate of an input signal to perform a phase synchronization control so that the input signal and an oscillation output have a constant phase difference and extracting a clock timing based on the transmission rate (figure 1 column 2 line 41 to column 3 line 35). Solheim and Turney are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock timing extraction circuit disclosed by Turney with the regeneration control circuit disclosed by Solheim. The suggestion/motivation for doing so would have been to reducing time delay in the synthesizer (Turney column 3 lines 18-28). Wada discloses determining whether signal logic levels measured at adjacent monitor points match with each other and to automatically measure a decision point within a valid zone of an eye pattern at which there is the least possibility that error occurs and performing the regeneration control by using the decision point as an optimal point (figures 7-10, column 10 lines 14-39). Solheim and Wada are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock recovery circuit disclosed by Wada with the regeneration control circuit disclosed by Solheim. The suggestion/motivation for

doing so would have been to produce a timing clock signal at a point at which an eye pattern of the signal opens most widely (Wada abstract).

As per claim 2, Solheim, Turney and Wada disclose claim 1, Turney also discloses that the clock timing extraction circuit comprises a phase comparing means for comparing phases of the input signal and a frequency-divided clock to detect a phase difference therebetween (figure 1 block 12 column 2 line 41 to column 3 line 35); averaging means for averaging the phase difference to generate a control voltage (figure 1 block 16 column 2 line 41 to column 3 line 35); voltage-controlled oscillation means for oscillating a synchronizing clock based on the control voltage (figure 1 block 18 column 2 line 41 to column 3 line 35); frequency-dividing means for dividing the frequency of the synchronizing clock to generate the frequency-divided clock (figure 1 block 14 column 2 line 41 to column 3 line 35); and phase-locked loop control means for determining whether the control voltage falls within a set range to determine whether a phase-locked loop is in a locked state and dynamically setting the frequency-dividing ratio based on a result of determination (figure 1 block 26 column 2 line 41 to column 3 line 35). Solheim and Turney are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock timing extraction circuit disclosed by Turney with the regeneration control circuit disclosed by Solheim. The suggestion/motivation for doing so would have been to reducing time delay in the synthesizer (Turney column 3 lines 18-28).

As per claim 5, Solheim, Turney and Wada disclose claim 1, Solheim also discloses that the regeneration control circuit comprises a voltage threshold level setting means for making a decision on the input signal by using the voltage threshold level and generating measured data from the input signal (figure 3 block 16 output 13 column 6 lines 5-17); clock phase setting means for setting a phase of the clock (figure 3 block 14 column 5 lines 48-54); level decision control means (figure 3 block 16 column 6 lines 5-17); decision information hold means for holding the decision information (figure 3 block 18 column 6 lines 5-17); and optimal point setting means for identifying a decision point within the valid zone of the eye pattern at which there is the least possibility that error occurs from the decision information obtained by sequentially sweeping the voltage threshold level and the extracted phase of clock and performing the regeneration control in which the decision point thus identified is used as the optimal point (figure 2 and figure 3 block 16 column 5 lines 55-62). Solheim doesn't specifically disclose determining whether signal logic levels of the measured data at the adjacent monitor points match with each other and providing the result of said determination as decision information. Wada discloses determining whether signal logic levels of the measured data at the adjacent monitor points match with each other and providing the result of said determination as decision information (figures 7-10, column 10 lines 14-39). Solheim and Wada are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock recovery circuit disclosed by Wada with the regeneration control circuit disclosed by Solheim. The suggestion/motivation for

doing so would have been to produce a timing clock signal at a point at which an eye pattern of the signal opens most widely (Wada abstract).

As per claim 6, Solheim, Turney and Wada disclose claim 5, Solheim also discloses that the level decision control means pulls in phase a first output of the measured data triggered by a current clock and a second output of the measured data triggered by a delayed clock obtained by delaying the current clock by a fixed time, makes an exclusive-OR operation on the first and second outputs to make a level decision on the monitor point and generates the decision information (figure 4 blocks 101-102 column 6 lines 36-53).

As per claim 7, Solheim, Turney and Wada disclose claim 5, Solheim also discloses that the optimal point setting means applies an offset adjustment control to the clock timing extraction circuit when a maximum transmission rate of the input signal is equal to the rate of the synchronizing clock to thereby generate a through clock, the clock phase setting means selects the through clock to sweep the clock phase (figure 3 column 5 lines 40-54).

As per claim 8, Solheim, Turney and Wada disclose claim 5, Solheim also discloses that the optimal point setting means applies a count value control and a digital phase step control to the clock phase setting means when the transmission rate of the input signal is lower than that of the synchronizing clock to thereby generate a clock signal having a different frequency-dividing ratio, and applies an offset adjustment control to the clock timing extraction circuit to thereby generate a frequency-divided

signal based on the clock signal, the clock phase setting means selects the frequency-divided clock to sweep the clock phase (figure 3 column 6 lines 5-17).

As per claim 9, Solheim, Turney and Wada disclose claim 5, Solheim also discloses that the optimal point setting means sets a reset cycle based on an error rate corresponding to the transmission rate of the input signal, and resets the decision information held in the decision information holding means on the basis of the reset cycle (figure 2 and figure 3 column 6 lines 18-26).

As per claim 10, Solheim, Turney and Wada disclose claim 9, Solheim also discloses that the optimal point setting means controls to shift a next monitor point without waiting for the reset cycle when recognizing that the decision information is indicative of error (figure 2 and figure 3 column 6 lines 36-53).

As per claim 11, Solheim, Turney and Wada disclose claim 5, Solheim also discloses that the optimal point setting means comprises a memory for memorizing the decision information about the monitor points, and determines, as the optimal point, a monitor point located in a memory area in which there is the least error with respect to the voltage threshold level and the clock phase (figure 3 block 18 column 6 lines 5-18).

As per claim 12, Solheim, Turney and Wada disclose claim 11, Solheim also discloses that the optimal point setting means memorizes the voltage threshold level and the clock phase at the monitor point determined as the optimal point, and performs the regeneration control using the memorized voltage threshold level and the clock phase at the time of restart (figure 3 column 6 lines 5-26).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solheim, Turney and Wada as applied to claim 2 above, and further in view of Nakamura (US 6741668). Solheim, Turney and Wada disclose claim 2. Solheim, Turney and Wada don't specifically disclose that the phase comparing means makes an exclusive-OR operation on a level of a rising edge of the frequency-divided clock and that of a falling edge thereof so that the phase difference is detected as a duty ratio. Nakamura discloses that the phase comparing means makes an exclusive-OR operation on a level of a rising edge of the frequency-divided clock and that of a falling edge thereof so that the phase difference is detected as a duty ratio (figure 7 column 3 line 37 to column 4 line 6 and column 13 lines 1-65). Solheim, Turney, Wada and Nakamura are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the exclusive-or operation circuit disclosed by Nakamura with the regeneration control circuit disclosed by Solheim, Turney and Wada. The suggestion/motivation for doing so would have been to reduce the jitter of the receiver (Nakamura column 2 lines 41-51).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solheim, Turney and Wada as applied to claim 2 above, and further in view of Itaya (US 4625180). Solheim, Turney and Wada disclose claim 2. Solheim, Turney and Wada don't specifically disclose that the phase-locked loop control means sets a frequency-dividing ratio available before power off in the frequency-dividing means at the time of power off and sets a control voltage available before breaking of the input signal in the averaging means when the input signal breaks. Itaya discloses that the phase-locked

loop control means sets a frequency-dividing ratio available before power off in the frequency-dividing means at the time of power off and sets a control voltage available before breaking of the input signal in the averaging means when the input signal breaks (figure 4 column 5 lines 40-50). Solheim, Turney, Wada and Itaya are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the power off technique disclosed by Itaya with the regeneration control circuit disclosed by Solheim, Turney and Wada. The suggestion/motivation for doing so would have been to reduce the fluctuations of the phase locked loop the receiver (Itaya abstract).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Solheim (US 5896391) in view of Wada (US 5602879 A). Solheim discloses a regeneration control circuit performing a regeneration control of an input signal, comprising a voltage threshold level setting means for making a decision on the input signal by using a voltage threshold level and generating measured data from the input signal (figure 3 block 16 output 13 column 6 lines 5-17); clock phase setting means for setting a phase of a clock for decision making (figure 3 block 14 column 5 lines 48-54); level decision control means (figure 3 block 16 column 6 lines 5-17); decision information hold means for holding the decision information (figure 3 block 18 column 6 lines 5-17); optimal point setting means for identifying a decision point within a valid zone of an eye pattern at which there is the least possibility that error occurs from the decision information obtained by sequentially sweeping the voltage threshold level and the phase of the clock with respect to the input signal and performing the regeneration control in which

the decision point thus identified is used as an optimal point (figure 2 and figure 3 block 16 column 5 lines 55-62); and that the regeneration control circuit performs the sweeping of the voltage threshold level and the phase of the extracted clock at intervals derived from a target error, rate of the input signal (column 6 lines 40-46). Specifically Solheim discloses "FIG. 4A is a flow chart of the operation of the control circuit in the error mapping mode. After control circuit 16 assumes the error mapping mode of operation, as shown in step 100, the threshold V_{th} and the phase Φ are initialized for BER contour mapping in step 101. T_{prov} defines the sampling time for measuring the current raw BER. Alternatively, rather than measuring the true current BER_{raw}, a shorter time interval T_{prov} may be set for limiting the collection time for each pair (V_i,. Φ_j). T_{prov} should be selected long enough to obtain a raw BER which is below the maximum admissible error rate BER_{prov}. Steps 102 to 108 illustrate the mapping process, wherein the slicing level V_i takes (I) successive values, and the phase Φ_j takes (J) successive values. In the example shown in FIG. 2, I=10 and J=16. All pairs (V_i,. Φ_j) are applied to the comparator 10 and flip-flop 12, respectively, in step 102, and the current raw BER is measured in step 103 for the time interval T_{prov}, as illustrated in step 104"0. Solheim doesn't specifically disclose determining whether signal logic levels of the measured data at the adjacent monitor points match with each other and providing the result of said determination as decision information. Wada discloses determining whether signal logic levels of the measured data at the adjacent monitor points match with each other and providing the result of said determination as decision information (figures 7-10, column 10 lines 14-39). Solheim and Wada are analogous art because they are from

the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock recovery circuit disclosed by Wada with the regeneration control circuit disclosed by Solheim. The suggestion/motivation for doing so would have been to produce a timing clock signal at a point at which an eye pattern of the signal opens most widely (Wada abstract).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naito (US 6538786) in view of Solheim (US 5896391), further in view of Turney (US 4516083 A) and further in view or Wada (US 5602879 A). Naito discloses an optical receiver receiving a light signal and performing a regeneration control, comprising an opto-electric conversion unit converting the light signal into an electric signal (figure 1 block 31 column 10 lines 40-51); a filtering unit performing a waveform equalizing control of the electric signal (figure 1 block 31 column 10 lines 40-51). Naito doesn't disclose a clock timing extraction unit dynamically setting a frequency-dividing ratio based on a transmission rate of the input signal to perform a phase synchronization control so that there is a fixed phase difference between the input signal and an oscillation output and extracting a clock timing based on the transmission rate; and a regeneration control unit sequentially sweeping a voltage threshold level and phase of the extracted clock with respect to the input signal to determine whether signal logic levels measured at adjacent points match with each other and based thereon finding an optimal point within a valid zone of an eye pattern at which there is the least possibility that error occurs. Turney discloses a clock timing extraction unit dynamically setting a frequency-dividing ratio based on a transmission rate of the input signal to perform a phase

synchronization control so that there is a fixed phase difference between the input signal and an oscillation output and extracting a clock timing based on the transmission rate (figure 1 block 14 column 2 line 41 to column 3 line 35). Naito and Turney are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock timing extraction circuit disclosed by Turney with the optical communication system disclosed by Naito. The suggestion/motivation for doing so would have been to reducing time delay in the synthesizer (Turney column 3 lines 18-28). Solheim discloses a regeneration control unit sequentially sweeping a voltage threshold level and phase of the extracted clock with respect to the input signal (figure 3 column 5 line 25 to column 6 line 35); and that the regeneration control circuit performs the sweeping of the voltage threshold level and the phase of the extracted clock at intervals derived from a target error, rate of the input signal (column 6 lines 40-46). Specifically Solheim discloses."FIG. 4A is a flow chart of the operation of the control circuit in the error mapping mode. After control circuit 16 assumes the error mapping mode of operation, as shown in step 100, the threshold V_{th} and the phase Φ are initialized for BER contour mapping in step 101. T_{prov} defines the sampling time for measuring the current raw BER. Alternatively, rather than measuring the true current BER_{raw}, a shorter time interval T_{prov} may be set for limiting the collection time for each pair (V_i,. Φ_j). T_{prov} should be selected long enough to obtain a raw BER which is below the maximum admissible error rate BER_{prov}. Steps 102 to 108 illustrate the mapping process, wherein the slicing level V_i takes (I) successive values, and the phase Φ_j takes

(J) successive values. In the example shown in FIG. 2, I=10 and J=16. All pairs (V_i,. Φ_j) are applied to the comparator 10 and flip-flop 12, respectively, in step 102, and the current raw BER is measured in step 103 for the time interval T_{prov}, as illustrated in step 104"). Naito, Turney and Solheim are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the data recovery system disclosed by Solheim with the optical communication system disclosed by Naito and Turney. The suggestion/motivation for doing so would have been to provide an optima operation point (Solheim abstract). Wada discloses determining whether signal logic levels of the measured data at the adjacent monitor points match with each other and providing the result of said determination as decision information (figures 7-10, column 10 lines 14-39). Naito, Turney, Solheim and Wada are analogous art because they are from the same field of endeavor. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate the clock recovery circuit disclosed by Wada with the optical communication system disclosed by Naito, Turney and Solheim. The suggestion/motivation for doing so would have been to produce a timing clock signal at a point at which an eye pattern of the signal opens most widely (Wada abstract).

Allowable Subject Matter

Claim 16 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
03-26-2007

TEMESGHEN GHEBRETINSAE
PRIMARY EXAMINER